WHAT IS CLAIMED IS:

1. An electrostatic discharge (ESD) protection circuit comprising:

first and second nodes:

a first thyristor having an anode connected to said first node, and a cathode and a gate both connected to said second node; and

a second thyristor having an anode connected to said second node, and a cathode and a gate both connected to said first node,

whereby said ESD protection circuit discharges an ESD curent, applied to said first node, toward said second node, and discharges an ESD current, applied to said second node, toward said first node.

2. The ESD protection circuit according to claim 1, wherein each of said first thyristor and said second thyristor has a four-region structure including a first well of a first conductivity type, a first diffusion region of a second conductivity type formed in said first well, said second conductivity type being opposite to said first conductivity type, a second well of said second conductivity type, and a second diffusion region of said first conductivity type formed in said second well.

3. The ESD protection circuit according to claim 1, wherein each of said first thyristor and said second thyristor has a four-region structure including a portion of a semiconductor substrate of a first conductivity type, a first diffusion region of a second conductivity type formed in said portion, a second well of said second conductivity type formed in said

semiconductor substrate, and a second diffusion region of said first conductivity type formed in said second well.

4. An ESD protection circuit formed on a semiconductor substrate of a first conductivity type, comprising:

first and second nodes;

a first well of a second conductivity type opposite to said first conductivity type, a second well of said second conductivity type disposed apart from said first well, and a third well of said first conductivity type encircling said first and second wells and connected to said first node, said first through third wells being formed in a surface region of said semiconductor substrate;

a first diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said third well to oppose said first well, and connected to said first node;

a second diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said third well to oppose said second well, and connected to said second node;

a third diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said first well, and connected to said first node;

a fourth diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said second well, and connected to said second node;

a fifth diffusion region of said first conductivity type, having a

higher impurity concentration than said third well, formed in said first well apart from said third well, and connected to second node; and

a sixth diffusion region of said first conductivity type, having a higher impurity concentration than said third well, formed in said second well apart from said fourth diffusion region, and connected to said first node.

5. The ESD protection circuit according to claim 4, wherein said first diffusion region has an edge opposing and extending parallel to an edge of said first well.

6. The ESD protection circuit according to claim 4, wherein said second diffusion region has an edge opposing and extending parallel to an edge of said second well.

7. The ESD protection circuit according to claim 4, wherein said fifth diffusion region is disposed between said first diffusion region and said third diffusion region.

8. The ESD protection device according to claim 4, said sixth diffusion region is disposed between said second diffusion region and said fourth diffusion region.

9. The ESD protection circuit according to claim 1, wherein said first node and said second node have a common potential during a normal

operation mode of a semiconductor device including said ESD protection device.

10. The ESD protection circuit according to claim 1, wherein said first and second conductivity types are P-type and N-type, respectively.

11. A semiconductor device comprising a plurality of separate power source systems, and at least one said ESD protection circuit according to claim 1, wherein said first and second nodes are connected to a ground line of one of said power systems and a ground line of another of said power systems, respectively.

12. An ESD protection circuit formed on a semiconductor substrate of a first conductivity type, comprising:

first and second nodes;

a first well of a second conductivity type opposite to said first conductivity type, a second well of said second conductivity type disposed apart from said first well, a third well of said first conductivity type encircling said first well and connected to said first node, and a fourth well of said first conductivity type encircling said second well, disposed apart from said third well and connected to said second node, said first through fourth wells being formed in a surface region of said semiconductor substrate;

a first diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said third well

to oppose said first well, and connected to said first node;

a second diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said fourth well to oppose said second well, and connected to said second node;

a third diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said first well, and connected to said first node;

a fourth diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said second well, and connected to said second node;

a fifth diffusion region of said first conductivity type, having a higher impurity concentration than said third well, formed in said first well apart from said third well, and connected to second node; and

a sixth diffusion region of said first conductivity type, having a higher impurity concentration than said fourth well, formed in said second well apart from said fourth diffusion region, and connected to said first node.

13. An ESD protection circuit formed on a semiconductor substrate of a first conductivity type, comprising:

first and second nodes;

a first well of a second conductivity type opposite to said first conductivity type, a second well of said second conductivity type disposed apart from said first well, a third well of said first conductivity type encircling said first well and connected to said first node, and a fourth well

of said first conductivity type encircling said second well, disposed apart from said third well and connected to said first node, said first through fourth wells being formed in a surface region of said semiconductor substrate;

a first diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said third well to oppose said first well, and connected to said first node;

a second diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said fourth well to oppose said second well, and connected to said second node;

a third diffusion region of said second conductivity type, having a higher impurity concentration than said first well, formed in said first well, and connected to said first node;

a fourth diffusion region of said second conductivity type, having a higher impurity concentration than said second well, formed in said second well, and connected to said second node;

a fifth diffusion region of said first conductivity type, having a higher impurity concentration than said third well, formed in said first well apart from said third well, and connected to second node; and

a sixth diffusion region of said first conductivity type, having a higher impurity concentration than said fourth well, formed in said second well apart from said fourth diffusion region, and connected to said first node